EDA Tools for RFIC Design: Business and Product News

Helic, Inc.—VeloceRF™ Qualified by TSMC

Helic, Inc. (www.helic.com) has announced that TSMC has qualified its VeloceRF tool as part of TSMC's Electromagnetic (EM) Tool Qualification Program. VeloceRF has been accuracy-certified against TSMC's 65nm silicon-verified spiral inductor set.
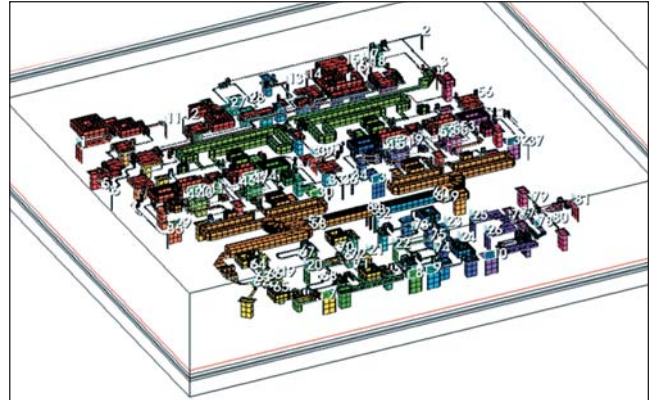
TSMC's EM Tool Qualification Program assists IC designers by providing certified process technology files, layout and measurements for 65 nm and 90 nm process technologies. The program ensures greater accuracy of EM simulators and extractors used in applications such as high-speed digital clock circuits and high-frequency mixed-signal RF designs. Certified process files eliminate several error sources in the design process and enable designers to use Helic's VeloceRF platform on TSMC 65 nm processes with confidence.

Helic's VeloceRF features a rapid and high-capacity, vector-based RLCK modeling engine that can generate very accurate models for any kind of integrated inductive component, and also includes a spiral inductor synthesizer. It eliminates the need for custom layout and eases adoption by foundries and design teams. Features such as conductor track slotting to mitigate metal stress, geometry resizing under current density constraints and the use of dummy fill patterns are pre-programmed in VeloceRF and are consistently supported by the layout and LVS modules.

AWR Corporation—PDK for WIN Semiconductors GaAs Foundry Process

AWR (www.awrcorp.com) and WIN Semiconductors Corporation (www.winfoundry.com) have announced the release of the WIN/AWR H2W PH50-00 process design kit (PDK). The PDK for the WIN PH50-00 GaAs enhancement/depletion-mode pseudomorphic high electron mobility transistor (pHEMT) and heterojunction bipolar transistor (HBT) foundry process is the latest in AWR's series of PDKs available for monolithic microwave integrated circuit (MMIC) designers.

WIN PH50-00 is a high-frequency, high-power MMIC process that has been in production since 2007. The new WIN/AWR PDK announced today fully exploits the process along with the unique technologies in the latest version of Microwave Office software (v2009), as well as AWR's ACE™ automatic circuit extraction technology, AXIEM™ 3D planar electromagnetic simulator, and APLAC® multi-rate harmonic balance simulator. The
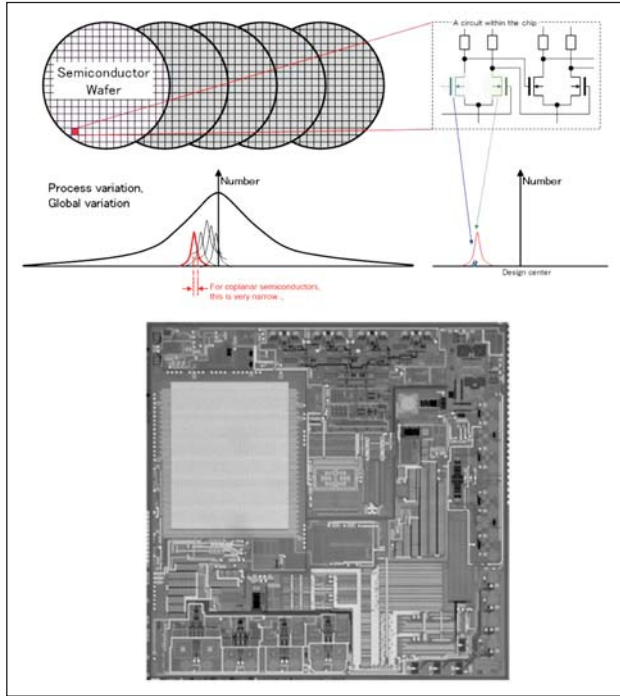

AWR's AXIEM was able to electromagnetically solve this mm-wave converter MMIC for Mimix Broadband.

WIN/AWR PP50-00 PDK can be resident in Microwave Office software simultaneously with packaging and other foundry PDKs to provide a complete module co-design environment. The AWR/WIN PH50-00 PDK is available for immediate use within AWR's Microwave Office v2009 software. All AWR/WIN PDKs are distributed by WIN and available free of charge to qualifying customers.

A recent "AWR Success Story" has been published, describing how Mimix Broadband (www.mimixbroadband.com) solved an entire MMIC chip using AWR's AXIEM 3D Planar EM Software. Mimix Broadband, Inc. supplies high performance gallium arsenide (GaAs) semiconductors from DC to 50 GHz for RF, microwave and millimeter-wave applications. Mimix was designing a mm-wave converter using an innovative design in the passive circuitry. If the design technique works the way Mimix believes, they can achieve very aggressive specs for system performance without having to use larger, conventional mm-wave structures. Only by solving the entire structure can Mimix designers verify their design ideas.

Using other solvers, Mimix was unable to electromagnetically (EM) simulate the entire monolithic microwave integrated circuit (MMIC) circuit, which includes more than 100 ports and 100k unknowns (see photo above), using other EM solvers and turned to AWR. As a result, AXIEM solved the entire structure on a desktop PC. With an electromagnetic solution for the full chip, Mimix could explore the circuit's physics and evaluate new mm-wave design methods.

Agilent's GoldenGate RFIC simulator provides features such as the process variation analysis depicted here

Agilent Technologies—PDKs for ADS 2009 and Jazz Semiconductor's 0.18 μm BiCMOS process

Agilent Technologies Inc. (www.agilent.com) recently announced the availability of two process design kits (PDKs) for Jazz Semiconductors (www.jazzsemi.com) 0.18-micron SiGe BiCMOS process offerings that are used with Agilent's Advanced Design System 2009 EDA software. The PDKs accelerate customers' time-to-market for IC development in automotive collision avoidance, high-data-rate networks, emerging HDTV wireless standards and other high-speed applications.

The Jazz SBC18HA and SBC18H2 PDKs are the result of collaboration between Jazz and Agilent to offer an accurate and productive work environment for the industry's latest SiGe MMIC design solutions. The SBC18HA and SBC18H2 have been widely accepted in many high-frequency applications, including 24 GHz and 77 GHz collision avoidance radar, 60 GHz WLAN HDTV, wireless base-station back haul, and a host of optical applications, including TIA, laser drivers, SERDES and CDRs.

Agilent also announced validation of its GoldenGate RFIC simulation, analysis and verification tool for STMicroelectronics' (www.st.com) 32 nm RF CMOS technology. The qualification of GoldenGate for ST's 32 nm RF technology is the result of a long-term collaboration between the two companies that includes 65 nm and other market-critical processes. Agilent's GoldenGate software (see figure above) is an advanced simulation and analysis solution for integrated mixed-signal RFIC designs. Its unique simulation algorithms are optimized for the demands of today's complex RFICs, and its capacity enables full characterization of complete transceivers, including parasitics, prior to tape-out.

Cadence Design Systems—Linear Technology Adopts Cadence for Integrated Design Flow

Cadence Design Systems, Inc. (www.cadence.com), announces that Linear Technology Corporation (www.linear.com), a supplier of high performance analog integrated circuits for communications, computer, automotive, and industrial companies worldwide, has adopted a broad range of Cadence Design Systems technologies as an integrated design flow. The new flow is expected to provide improved analog and mixed signal simulation and layout capabilities for faster design time and higher accuracy.

Key components of the integrated flow include Cadence's Virtuoso® Analog Design Environment, Virtuoso AMS Designer Simulator, Virtuoso Multi-Mode Simulation, Assura® Design Rule Checker, Assura Layout vs. Schematic Verifier, and QRC Extraction.

Cadence also announced that it has developed a protocol testing solution using instrumentation from Rohde & Schwarz (www.rohde-schwarz.com) that enables early validation of next-generation 4G/LTE wireless SoC/ASIC designs. The solution integrates the Cadence Incisive® Palladium® accelerator/emulator and the R&S CMW500 LTE network emulator, allowing wireless/mobile companies to test their complex designs much earlier than when silicon becomes available.

PSP Models Help NXP and TSMC Deliver 45 nm Single-Chip Digital TV Platform

With the newly introduced DTV platform allowing TV viewers to enjoy HD digital content and Internet access with unparalleled picture quality, NXP Semiconductors (www.nxp.com) and Taiwan Semiconductor Manufacturing Company, Ltd. (www.tsmc.com) have announced their cooperation in the development of the industry's first single-chip 45 nm global LCD TV platform, TV550. NXP and TSMC have reached a major milestone in enabling the next generation of mainstream digital TV sets for TV manufacturers. NXP is now delivering engineering samples to key customers.

Featuring NXP's PNX85500 processor, built on TSMC's 45 nm low power process technology, the NXP TV550 digital TV platform is a production-ready reference design that reduces time-to-market and reduces costs with its high level of functional integration. The long-term partnership and collaboration between NXP and TSMC was the key to this first-to-market achievement, with early access to silicon test results from TSMC resulting in accurate transistor characterization using state-of-the art PSP (Pennsylvania State University-Philips) models.

Next month's Technology Report will focus on technology developments that target military applications—communications, navigation, sensors, radar, countermeasures.